





United States Patent and Trademark Office

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.	
10/040,745	01/07/2002	John S. Kresge	END919970075US3	4111	
75	590 11/26/2002				
IBM Corporation / IP Law N50/040-4			EXAMINER		
1701 North Stree Endicott, NY			NGUYEN, D	NGUYEN, DONGHAI D	
			ART UNIT	PAPER NUMBER	
			3729 DATE MAILED: 11/26/2002	H	

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)				
Office Action Summer	10/040,745	KRESGE ET AL.				
Office Action Summary	Examiner	Art Unit				
	Donghai D. Nguyen	3729				
The MAILING DATE of this communication appears on the cover sheet with the correspondence address Period for Reply						
A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION. - Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication. - If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely. - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication. - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). - Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b). Status						
1) Responsive to communication(s) filed on 07	January 2002 .					
2a) ☐ This action is FINAL. 2b) ☑ The	nis action is non-final.					
3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under <i>Ex parte Quayle</i> , 1935 C.D. 11, 453 O.G. 213. Disposition of Claims						
4)⊠ Claim(s) <u>80-97</u> is/are pending in the application.						
4a) Of the above claim(s) is/are withdrawn from consideration.						
5) Claim(s) is/are allowed.						
6)⊠ Claim(s) <u>80-97</u> is/are rejected.						
7) Claim(s) is/are objected to.						
8) Claim(s) are subject to restriction and/or election requirement.						
Application Papers						
9) The specification is objected to by the Examiner.						
10)⊠ The drawing(s) filed on <u>07 January 2002</u> is/are: a)□ accepted or b)⊠ objected to by the Examiner.						
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).						
11) The proposed drawing correction filed on is: a) approved b) disapproved by the Examiner.						
If approved, corrected drawings are required in reply to this Office action.						
12) The oath or declaration is objected to by the Examiner.						
Priority under 35 U.S.C. §§ 119 and 120						
13) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).						
a) All b) Some * c) None of:						
1. Certified copies of the priority documents have been received.						
2. Certified copies of the priority documents have been received in Application No						
3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)). * See the attached detailed Office action for a list of the certified copies not received.						
14) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).						
a) ☐ The translation of the foreign language provisional application has been received. 15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.						
Attachment(s)						
1) Notice of References Cited (PTO-892) 2) Notice of Draftsperson's Patent Drawing Review (PTO-948) 3) Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2	5) Notice of Informa	rry (PTO-413) Paper No(s) I Patent Application (PTO-152)				
U.S. Patent and Trademark Office PTO-326 (Rev. 04-01) Office A	ction Summary	Part of Paper No. 4				

Art Unit: 3729

DETAILED ACTION

Drawings

1. The drawings are objected to because the reference number "26" is pointed to a different part in Fig. 1. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

2. The disclosure is objected to because of the following informalities: on page 16, line 9 the word "pads 103" should be --pads 103--.

Appropriate correction is required.

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: "METHOD OF MAKING THE ELECTRONIC PACKAGE".

4. The abstract of the disclosure is objected to because the claimed inventions are method claims. Correction is required. See MPEP § 608.01(b).

Claim Rejections - 35 USC § 112

- 5. The following is a quotation of the second paragraph of 35 U.S.C. 112:
 - The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.
- 6. Claims 82 and 88-89 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The phrase "Laminating ... dielectric layers" (claim 82, line 4) is vague; examiner does not know how one copper foil being laminated onto two separated dielectric layers.

The phrase "said third dielectric layer" (claim 88, line 4) lacks of antecedent basis. Examiner notices that this layer has not been formed.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

- (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
- 8. Claims 80, 82-87, 91, and 93-97 are rejected under 35 U.S.C. 102(b) as being anticipated by US Patent 4,882,454 to Peterson et al.

Regarding claim 80, Peterson et al. disclose a method of making a multi-layer interconnect structure, the method comprising: providing a thermally conductive layer (102); positioning first (310) and second (311) dielectric layers on the thermally conductive layer; and position first (312) and second (313) pluralities of electrically conductive members on the first and second dielectric layers, each of said first and second pluralities of electrically conductive members adapted for having solder connection (103 and 104) thereon, and the thermally conductive layer being comprised of material having selected thickness and coefficient of thermal expansion (Col. 2, lines 40-53).

Regarding to claims 82 and 93, Peterson et al. disclose laminating a copper foil (105) onto the first and second dielectric layers (101); etching (Col. 2, lines 19-21) selected portion of copper foil to produce first and second pluralities of electrical conductive member (312, 313) of electrically conductive members (Fig. 4).

Regarding claims 83, 85, 94 and 96, see figure 1.

Regarding claims 84, 86, 95, and 97, the portions of third and fourth dielectric layer are removed by laser ablating (Col. 3, line 26).

Regarding claim 87, Peterson et al. disclose a method of making an electronic package comprising the steps of: providing a semiconductor chip (Col. 2, lines 2-3); providing a multi-layered interconnect structure (Fig. 1) including a thermally conductive layer (102), a first (310) and second (311) dielectric layers on the thermally conductive layer, and a first (312) and second (313) pluralities of electrically conductive members on the first and second dielectric layers; providing a first plurality of solder connections on the first plurality of electrically conductive members; and connecting the first plurality of electrically conductive to plurality of contact sites on the chip (Col. 2, lines 1-3), and the thermally conductive layer being comprised of material having selected thickness and coefficient of thermal expansion (Col. 2, lines 40-53).

Regarding claim 91, Peterson et al. disclose a method of making a multi-layer interconnect structure, the method comprising: providing a thermally conductive layer (102); positioning first (101, 310) and second (101, 311) dielectric layers on the thermally conductive layer; positioning first electrically conductive layer (105, 312) within the first dielectric layer; positioning a second electrically conductive layer (302) between the first electrically conductive layer (105, 312) and thermally conductive layer (102); and position first (105) and second (105) pluralities of electrically conductive members(Fig. 1) on the first and second dielectric layers (101), each of said first and second pluralities of electrically conductive members adapted for

having solder connection (103 and 104) thereon, and the thermally conductive layer being comprised of material having selected thickness and coefficient of thermal expansion (Col. 2, lines 40-53).

Claim Rejections - 35 USC § 103

- 9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:
 - (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
- 10. Claims 81, 88, and 92 are rejected under 35 U.S.C. 103(a) as being unpatentable over Peterson et al.

Regarding claims 81 and 92, Peterson et al. disclose the step of laminating except for the specific range of temperature and pressure. At the time the invention was made it would have been obvious matter of design choice to one having ordinary skill in the art to specify a specific range of temperature and pressure in the step of lamination because Applicant have not disclose that the specific temperature and pressure provide an advantage, are used for a particular purpose, or solve a stated problem. One ordinary skill in the art would have expected Applicants' invention to perform equally well as Peterson et al.'s invention. Therefore, it would have been obvious matter of design choice to specify a specific range of temperature and pressure in the step of laminating the first and second dielectric layers onto the thermally conductive layer to obtain the invention as specified in claims 81 and 92.

Regarding claim 88, Peterson et al. disclose forming a plurality of open in third dielectric layer (Fig. 1) that exposing a portion of the first plurality of electrically conductive members;

Page 6

Application/Control Number: 10/040,745

Art Unit: 3729

plating a conductive layer to form a plurality of microvias (106, 107; etc.), but Peterson et al. do not disclose step of applying and re-flowing a first solder paste. It would have been obvious matter of design choice to one having ordinary skill in the art at the time the invention was made to apply and re-flow a first solder paste onto the conductive layer because Applicant have not disclose that the steps of applying and re-flowing a first solder paste onto the conductive layer provide an advantage, are used for a particular purpose, or solve a stated problem. One ordinary skill in the art would have expected Applicants' invention to perform equally well with either without applying and re-flowing a first solder paste onto the conductive layer as taught by Peterson et al. or with claimed invention. Therefore, it would have been obvious matter of design choice to modify Peterson et al. to obtain the invention as specified in claim 88.

11. Claims 89 and 90 are rejected under 35 U.S.C. 103(a) as being unpatentable over Peterson et al. in view of US Patent 5,691,041 to Frankeny et al.

Regarding claim 89, Peterson et al. disclose the claim invention except for applying a second solder paste on solder connection, positioning the contact member of semiconductor chip against solder connection, and reflowing second solder paste to electrically connect said semiconductor chip to the multi-layer interconnect structure. However, Frankeny et al. disclose those steps (Fig. 6 and Col. 1, lines 43-50). It would have been obvious to one having ordinary skill in the art at the time the invention was made to add the steps of applying a second solder paste on solder connection, positioning the contact member of semiconductor chip against solder connection, and reflowing second solder paste to Peterson et al.'s method for electrically connecting said semiconductor chip to the multi-layer interconnect structure as taught by Frankeny et al.

Application/Control Number: 10/040,745

Art Unit: 3729

Page 7

solder connection (104) for connect to surface mounting device not to a circuitized substrate;

Regarding claim 90, Peterson et al. disclose the step of proving a second plurality of

however, Frankeny et al. shows a circuitized substrate (10) connecting with second plurality of

solder connections (Fig. 6). It would have been obvious to one having ordinary skill in the art at

the time the invention was made to provide the circuitized substrate as taught by Frankeny et al

for connecting Peterson et al.'s second plurality of solder connection to a Frankeny et al.'s circuit

board, in order to obtain the claimed invention.

Conclusion

Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Donghai D. Nguyen whose telephone number is (703) 305-7859.

The examiner can normally be reached on Monday-Friday (8:30-5:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Peter Vo can be reached on (703) 308-1789. The fax phone numbers for the

organization where this application or proceeding is assigned are (703) 305-7307 for regular

communications and (703) 305-3579 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding

should be directed to the receptionist whose telephone number is (703) 308-1148.

ARL J. ARBES

PRIMARY EXAMINER

DN

November 21, 2002